In the Claims

1. (currently amended) A Mask ROM, comprising:

a substrate~~s~~;

a plurality of gates on the substrate;

a gate oxide layer between the gates and the substrate;

a plurality of buried bit lines in the substrate between the gates;

an insulator on the buried bit lines and between the gates;

a plurality of word lines over the substrate perpendicular to the buried bit lines, wherein each word line is located over a row of gates and the insulator; ~~and~~ and

a coding layer between the word lines and the gates ~~constituting a plurality of memory cells~~, wherein

a gate, the substrate, the gate oxide layer under the gate, and the coding layer on the gate constitute a memory cell, and the coding layer on the gate of a memory cell serves as a coding region of the memory cell; and

the coding regions of some memory cells are implanted with coding ions and are in a logic state of 1 (or 0), and the coding regions of ~~the~~ other memory cells are not implanted with coding ions and are in a logic state of 0 (or 1).

2. (original) The Mask ROM of claim 1, wherein the coding layer comprises a semiconductor material.

3. (original) The Mask ROM of claim 2, wherein the semiconductor material includes undoped polysilicon.

4. (original) The Mask ROM of claim 1, wherein the word lines comprise doped polysilicon.

5. (original) The Mask ROM of claim 1, wherein the coding ions comprise PH_3 ions.

6. (original) The Mask ROM of claim 1, wherein the insulator comprises silicon oxide.